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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,162	03/31/2004	Stephen Wu	BP 3112	8187

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EXAMINER	
NGUYEN, HIEP	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,162	WU, STEPHEN	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-13,16-21,24 and 25* is/are allowed.

6)☒ Claim(s) *1,5,8,14,15,22,23,26-28 and 30-35* is/are rejected.

7)☒ Claim(s) *2-4,6,7,9 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03-31-04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MY-TRANG NU TON
PRIMARY EXAMINER
9/15/05

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Abstract

The Abstract is objected to because it is too long, over 150 words.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 14, 15, 22, 23 and 30-35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claims 14 and 22, the recitation "wherein, the first and second divider blocks are biased for digital operation" is indefinite because it is not clear what "bias for digital operation" is. Figure 4 of the present application shows no biasing scheme for biasing of the pre-scaled divider and the first and second divider blocks.

Regarding claim 30, the recitation "a multi-modulus divider module for producing a divided oscillation based upon an oscillation produced by a frequency source and a modulus control signal" on line 3 is indefinite because it is misdescriptive. Figure 3 of the present application shows that the "multi –modulus divider module" (112) receives only the oscillation (132) from the VCO. No modulus control signal is seen.

Regarding claim 31, the recitation "wherein the first latching block is biased by a first bias signal and wherein the second latching block is biased by a second bias signal, which second bias signal is greater in magnitude than the first bias signal" is indefinite because it is misdescriptive. Figure 3 of the present application shows that the first and second latching blocks are biased by a same "first bias signal".

Regarding claim 35, the recitation " wherein the second latching block is clocked by the frequency source oscillation and the first latching block is clocked by the buffered oscillation" is indefinite because it is misdescriptive. Figure 5 of the present application

shows that the second latching block (124) is clocked by the buffered oscillation (194) and the first latching block (120) is clocked by the pre-scaled divider output (152).

Claims 15, 23 and 32-34 are indefinite because of the technical deficiencies of claims 14, 22 and 30.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 5, 26, 30, 31 and 33 are rejected under 35 U.S.C.102 (b) as being anticipated by Lee et al. (USP. 6,424,192).

Regarding claim 1, figure 5 shows a phase-locked loop comprising: a phase detector (PFD); a charge pump (Chrg.Pump); a VCO (CMOS VCO); a low-noise divider (500) including a pulse-swallow divider (510, DFF0, DFF1); first to third latching blocks (DFF2, DFF3, DFF4).

Regarding claim 5, the pulse-swallow comprises a pre-scaled divider block (512), first and second divider blocks (DFF0, DFF1). Note that first and second divider blocks (DFF0, DFF1) are flip-flops biased for digital operation.

Regarding claim 26, figure 5 of Lee shows a method for producing a low-noise divided oscillation, comprising:

latching (Latch DFF0) a divided signal based upon a pre-scaled divider (512, 514,) output to produce a first latched signal wherein the pre-scaled divider output is based upon an oscillation (LO[0]);

latching the first latched signal based upon the oscillation to produce a second latched signal (output of latch DFF1);

latching the second latched signal (latch DFF2) based upon the oscillation to produce the low- noise divided oscillation.

Regarding claims 30 and 31, figure 5 of Lee shows a divider for producing a low phase noise divided oscillation, comprising:

a multi-modulus divider module (512, 514, DFF0, DFF1) for producing a divided oscillation based upon an oscillation produced by a frequency source (CMOS VCO) and a modulus control signal (P, S);

a first latching block (DFF2) for latching the divided oscillation based upon the frequency source oscillation (LO[2]) as a clock to produce a first latched signal; and a second latching block (DFF3) for latching the first latched signal based upon the frequency source oscillation (LO[3]) as a clock to produce a second latched signal, which second latched signal is the low phase noise divided oscillation. The first and second latching blocks are biased by a same bias signal.

Regarding claim 33 the plurality of divider blocks are elements (512, DFF0, DFF1). Note that flip-flops (DFF0, DFF1) each performs as a divide-by-2 circuit. The first and second latching blocks are biased by the frequency source oscillation (VCO).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8, 27, 28, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (USP. 6,424,192) in view of Johnson et al. (USP. 6,707,305).

Regarding claims 8, 27, 28 and 34, figure 5 of Lee includes all the limitations of these claims except for the limitation that there is a buffer coupled between the VCO and the low noise divider. Figure 3 of Johnson shows a buffer (104) for protecting the circuit coupled to the output of the buffer against over voltages and over current. Therefore, it would have been obvious to an artisan having skills in the art to implement a buffer circuit taught by Johnson between the VCO and the divider (500) for providing protection against over voltages and

over current. Regarding claim 28, the first and second latching blocks perform latching function with a first bias level.

Regarding claim 35, figure 5 of Chien shows that the first latch block (182) is clocked by the frequency source oscillation and the second latching block (172) is clocked by the buffered oscillation.

Allowable Subject Matter

Claims 2-4, 6, 7, 9 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 14, 15, 22, 23, 32 and 35 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claims 10-13, 16-21, 24 and 25 are allowed.

Claims 10-13, 16-21, 24 and 25 are allowed because the prior art of record fails to teach or suggest a divider comprising a pulse-swallow for producing a pre-scaled divider output and a divided oscillation as called for in claim 10; a method for producing a low phase noise divided oscillation comprising latching the divided oscillation based upon the pre-scaled divider output as a clock to produce a first latched signal as called for in claim 18.

Claims 2-4, 6, 7, 9 and 29 are objected to because the prior art of record fails to teach or suggest a phase-locked loop comprising first and second latching blocks that are biased by a first bias signal and a third latching block biased by a second bias signal as called for in claims 2 and 29;

Claims 14, 15, 22, 23, 32 and 35 would be allowable because the prior art of record fails to teach or suggest a pulse swallow comprising a pre-scaled divider block biased by the first bias signal as called for in claims 14 and 22.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
09-14-05

MY-TRANG NU TON
PRIMARY EXAMINER
9/16/05